IN THE CLAIMS:

Please cancel claim 2 in its entirety without prejudice nor disclaimer of the subject matter set forth therein and amend claims 1, 3, 4, 5, 7 and 9 as follows.

1. (Currently Amended) A method for driving a semiconductor memory,

said semiconductor memory containing:

a memory cell block including a plurality of ferroelectric capacitors successively connected to one another ~~along a bit line direction~~ each for storing a data in accordance with displacement of polarization of a ferroelectric film thereof and a reading transistor whose gate is connected to one end of said plurality of successively connected ferroelectric capacitors for reading a data by detecting the displacement of the polarization of said ferroelectric film of a selected ferroelectric capacitor selected from said plurality of ferroelectric capacitors;

a set line connected to the other end of said plurality of successively connected ferroelectric capacitors;

a bit line connected to a drain of said reading transistor at one end thereof;

a reset line connected to a source of said reading transistor at one end thereof; and

a plurality of word lines respectively corresponding to said plurality of ferroelectric capacitors and provided perpendicularly to said bit line for selecting said selected ferroelectric capacitor,

wherein voltages applied to said set line, and said reset line ~~and said word lines in selecting said selected ferroelectric capacitor or~~ for writing or erasing a data in said selected ferroelectric capacitor are a power voltage or a ground voltage.

2. (Canceled)

3. (Currently Amended) A method for driving a semiconductor memory,

said semiconductor memory containing:

a memory cell block including a plurality of ferroelectric capacitors successively connected to one another ~~along a bit line direction~~ each for storing a data in accordance with displacement of polarization of a ferroelectric film thereof and a reading transistor whose gate is connected to one end of said plurality of successively connected ferroelectric capacitors for reading a data by detecting the displacement of the polarization of said ferroelectric film of a selected ferroelectric capacitor selected from said plurality of ferroelectric capacitors;

a set line connected to the other end of said plurality of successively connected ferroelectric capacitors;

a bit line connected to a drain of said reading transistor at one end thereof;

a reset line connected to a source of said reading transistor at one end thereof; and

a plurality of word lines respectively corresponding to said plurality of ferroelectric capacitors and provided perpendicularly to said bit line for selecting said selected ferroelectric capacitor,

wherein a step of writing a data in said selected ferroelectric capacitor includes sub-steps of:

causing a potential difference obtained by subtracting a ground voltage <u>applied to said resent line</u> from a power voltage <u>applied to said set line</u> between an upper electrode and a lower electrode of said selected ferroelectric capacitor ~~by applying the power voltage to said set line and applying the ground voltage to said reset line~~, whereby turning the polarization of said ferroelectric film of said selected ferroelectric capacitor to a direction of

potential gradient of said potential difference; and

after causing said potential difference, removing said potential difference caused between the upper electrode and the lower electrode of said selected ferroelectric capacitor by applying the ground voltage to said set line.

4. (Currently Amended) A method for driving a semiconductor memory,

said semiconductor memory containing:

a memory cell block including a plurality of ferroelectric capacitors successively connected to one another ~~along a bit line direction~~ each for storing a data in accordance with displacement of polarization of a ferroelectric film thereof and a reading transistor whose gate is connected to one end of said plurality of successively connected ferroelectric capacitors for reading a data by detecting the displacement of the polarization of said ferroelectric film of a selected ferroelectric capacitor selected from said plurality of ferroelectric capacitors;

a set line connected to the other end of said plurality of successively connected ferroelectric capacitors;

a bit line connected to a drain of said reading transistor at one end thereof;

a reset line connected to a source of said reading transistor at one end thereof; and

a plurality of word lines respectively corresponding to said plurality of ferroelectric capacitors and provided perpendicularly to said bit line for selecting said selected ferroelectric capacitor,

wherein a step of erasing a data written in said selected ferroelectric capacitor includes sub-steps of:

causing a potential difference obtained by subtracting a power voltage from a

ground voltage between an upper electrode and a lower electrode of said selected ferroelectric capacitor by applying the ground voltage to said set line and applying the power voltage to said reset line, whereby turning the polarization of said ferroelectric film of said selected ferroelectric capacitor to a direction of potential gradient of said potential difference; and

after causing said potential difference, removing said potential difference caused between the upper electrode and the lower electrode of said selected ferroelectric capacitor by applying the ground voltage to said reset line.

5. (Currently Amended) A method for driving a semiconductor memory,

said semiconductor memory containing:

a memory cell block including a plurality of ferroelectric capacitors successively connected to one another ~~along a bit line direction~~ each for storing a data in accordance with displacement of polarization of a ferroelectric film thereof and a reading transistor whose gate is connected to one end of said plurality of successively connected ferroelectric capacitors for reading a data by detecting the displacement of the polarization of said ferroelectric film of a selected ferroelectric capacitor selected from said plurality of ferroelectric capacitors;

a set line connected to the other end of said plurality of successively connected ferroelectric capacitors;

a bit line connected to a drain of said reading transistor at one end thereof;

a reset line connected to a source of said reading transistor at one end thereof; and

a plurality of word lines respectively corresponding to said plurality of ferroelectric capacitors and provided perpendicularly to said bit line for selecting said selected ferroelectric capacitor,

wherein a step of reading a data from said selected ferroelectric capacitor includes sub-step of:

applying a power voltage to said bit line and a ground voltage to said reset line, or applying the ground voltage to said bit line and the power voltage to said reset line, and detecting voltage change caused on said bit line by applying a reading voltage to said set line; ~~and~~

after detecting said voltage change, removing a potential difference caused between an upper electrode and a lower electrode of said selected ferroelectric capacitor by applying the ground voltage to said set line; and

said reading voltage is set to such magnitude that said potential difference does not exceed a coercive voltage of said selected ferroelectric capacitor.

6. (Original) The method for driving a semiconductor memory of claim 5, further comprising, after the sub-step of removing said potential difference, a sub-step of turning off said reading transistor.

7. (Currently Amended) A method for driving a semiconductor memory,

said semiconductor memory containing:

a memory cell block including a plurality of ferroelectric capacitors successively connected to one another ~~along a bit line direction~~ each for storing a data in accordance with displacement of polarization of a ferroelectric film thereof and a reading transistor whose gate is connected to one end of said plurality of successively connected ferroelectric capacitors for reading a data by detecting the displacement of the polarization of said ferroelectric film of a selected ferroelectric capacitor selected from said plurality of ferroelectric capacitors;

a set line connected to the other end of said plurality of successively connected

ferroelectric capacitors;

a bit line connected to a drain of said reading transistor at one end thereof and to one end of a load resistance at the other end thereof;

a reset line connected to a source of said reading transistor at one end thereof; and

a plurality of word lines respectively corresponding to said plurality of ferroelectric capacitors and provided perpendicularly to said bit line for selecting said selected ferroelectric capacitor,

wherein a step of reading a data from said selected ferroelectric capacitor includes sub-step of:

applying a power voltage to the other end of said load resistance and a ground voltage to said reset line, or applying the ground voltage to the other end of said load resistance and the ~~ground~~ power voltage to said reset line, and comparing, with a reference voltage, voltage change caused at both ends of said load resistance owing to a current flowing between the drain and the source of said reading transistor ~~in~~ by applying a reading voltage to said set line; and

after comparing said voltage change, removing a potential difference caused between an upper electrode and a lower electrode of said selected ferroelectric capacitor by applying the ground voltage to said set line.

8. (Original) The method for driving a semiconductor memory of claim 7, further comprising, after the sub-step of removing said potential difference, a sub-step of turning off said reading transistor.

9. (Currently Amended) The method for driving a semiconductor memory of claim 7,

wherein said semiconductor memory further includes:

a second memory cell block having the same configuration as said memory cell block and disposed on a side of said memory cell block along a word line direction; and

a second bit line connected, at one end thereof,

to a drain of a second reading transistor included in said second memory cell block and connected, at the other end thereof, to one end of a second load resistance,

said set line is connected to the other end of a plurality of ferroelectric capacitors included in said second memory cell block,

said reset line is connected to a source of said second reading transistor included in said second memory cell block, and

said reference voltage corresponds to voltage change caused at both ends of said second load resistance owing to a current flowing between the drain and the source of said second reading transistor in applying the power voltage to the other end of said second load resistance and the ground voltage to said reset line, or applying the ground voltage to the other end of said second load resistance and the ~~ground~~ power voltage to said reset line, and applying the reading voltage to said set line.